WHAT IS CLAIMED IS:

Sub Cl

1. A semiconductor device comprising:

a substrate having at least one driving circuit comprising a plurality of thin film transistors and clock lines for supplying clock signals to the driving circuit,

wherein each of the clock lines or each of base portions of the clock lines is made of a two-layer structure, a lower layer of said two-layer structure comprising the same wiring material as gate electrodes of the thin film transistors and, an upper layer of said two-layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors.

2. A device according to claim 1, wherein an interval between adjacent ones of the clock lines is wider than a width of each of the clock lines.

3. A device according to claim 1, wherein said clock lines are connected to a shift register circuit in the driving circuit.

4. A device according to claim 1, further comprising a pixel portion comprising a plurality of thin film transistors on said substrate.

5. A semiconductor device comprising:

a substrate having at least one driving circuit comprising a plurality of thin film transistors, and clock lines for supplying clock signals to the driving circuit, black matrices over the thin film transistors, and wiring lines crossing the clock lines or the base portions of the clock lines,

wherein said wiring lines comprises the same layer as the black matrices.

6. A device according to claim 5, wherein each of the clock lines or each of base portions of the clock lines is made of a two-layer structure, a lower layer of said two-layer structure comprising the same wiring material as gate electrodes of the thin film transistors and, an upper layer of said two-layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors.

7. A device according to claim 5, wherein an interval between adjacent ones of the clock lines is wider than a width of each of the clock lines.

8. A device according to claim 5, wherein said clock lines are connected to a shift register circuit in the driving circuit.

9. A device according to claim 5, further comprising a pixel portion comprising a plurality of thin film transistors on said substrate.

10. A semiconductor device comprising:

a substrate having at least one driving circuit comprising a plurality of thin film transistors, and clock lines for supplying clock signals to the driving circuit, and at least one shielding line biased at a fixed potential,

wherein said shielding line is disposed on an interval between the clock lines.

11. A device according to claim 10, wherein each of the clock lines or each of base portions of the clock lines is made of a two-layer structure, a lower layer of said two-layer structure comprising the same wiring material as gate electrodes of the thin film transistors and, an upper layer of said two-layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors.

12. A device according to claim 10, wherein said wiring lines comprises the same layer as the black matrices.

13. A device according to claim 10, wherein an interval between adjacent ones of the clock lines is wider than a width of each of the clock lines.

14. A device according to claim 10, wherein said clock lines are connected to a shift register circuit in the driving circuit.

15. A device according to claim 10, further comprising a pixel portion comprising a plurality of thin film transistors on said substrate.

16. A semiconductor device comprising:

a substrate having at least one driving circuit comprising thin film transistors, signal lines for supplying signals to the driving circuit,

wherein each of the signal lines or each of base portions of the signal lines is made of a two-layer structure, a lower layer of said two-layer structure comprising the same wiring material as gate electrodes of the thin film transistors and, an upper layer of said two-layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors.

17. A device according to claim 16, wherein an interval between adjacent ones of the signal lines is wider than a width of each of the signal lines.

18. A device according to claim 16, wherein said signal lines are connected to an analog switch circuit in the driving circuit.

19. A device according to claim 16, further comprising a pixel portion comprising a plurality of thin film transistors on said substrate.

20. A semiconductor device comprising:

a substrate having at least one driving circuit comprising thin film transistors, signal lines for supplying signals to the driving circuit, black matrices over the thin film transistors, and wiring lines crossing the video signal lines or the base portions of the video signal lines;

wherein each of the signal lines or each of base portions of the signal lines is made of a two-layer structure, a lower layer of said two-layer structure comprising the same wiring material as gate electrodes of the thin film transistors and, an upper layer of said two-layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors, and

wherein said wiring lines are made of the same layer as the black matrices.

21. A device according to claim 20, wherein an interval between adjacent ones of the signal lines is wider than a width of each of the signal lines.

22. A device according to claim 20, wherein said signal lines are connected to an analog switch circuit in the driving circuit.

23. A device according to claim 20, further comprising a pixel portion comprising a plurality of thin film transistors on said substrate.

24. A semiconductor device comprising:

a substrate having at least one driving circuit comprising thin film transistors, signal lines for supplying signals to the driving circuit, and at least one shielding line biased at a fixed potential,

wherein said shielding line is disposed on an interval between the signal lines.

25. A device according to claim 24, wherein each of the signal lines or each of base portions of the signal lines is made of a two-layer structure, a lower layer of said two-layer structure comprising the same wiring material as gate electrodes of the thin film transistors and, an upper layer of said two-layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors.

26. A device according to claim 24, wherein said wiring lines are made of the same layer as the black matrices.

27. A device according to claim 24, wherein an interval between adjacent ones of the signal lines is wider than a width of each of the signal lines.

28. A device according to claim 24, wherein said signal lines are connected to an analog switch circuit in the driving circuit.

29. A device according to claim 24, further comprising a pixel portion comprising a plurality of thin film transistors on said substrate.